THE HONORABLE JAMES L. ROBART

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

MICROSOFT CORPORATION,

Plaintiff,

vs.

MOTOROLA, INC., et al.,

Defendants.

MOTOROLA MOBILITY, INC., et al.,

Plaintiffs,

vs.

MICROSOFT CORPORATION,

Defendants.

Case No. C10-1823-JLR

MICROSOFT CORPORATION'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY

NOTED: Friday, April 13, 2012

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The asserted apparatus claims of the patents in suit are invalid as indefinite because the patents do not adequately describe structure corresponding to the "means for decoding" and "means for using" elements. Instead, the patents disclose only general purpose computing devices for implementing the functions claimed in these means plus function claim elements. A general purpose computing device, however, does not qualify as structure corresponding to a means plus function claim element. Disclosing such a general purpose computing device requires also disclosing an algorithm for performing the claimed function. Here, the patents disclose no algorithm for performing the functions claimed in the "means for decoding" and "means for using" elements. Indeed, MMI has never identified an algorithm that allegedly performs these functions. The asserted apparatus claims are therefore invalid under 35 U.S.C. § 112, ¶ 2 for indefiniteness.

I. BACKGROUND

Motorola Mobility, Inc. ("MMI") has asserted that Microsoft infringes U.S. Patents 7,310,374; 7,310,375; and 7,310,376 (the "'374," "'375," and "'376" Patents, respectively), each entitled "Macroblock Level Adaptive Frame/Field Coding For Digital Video Content." All three patents share the same specification ("the common specification").[1] MMI asserts, *inter alia*, that Microsoft infringes independent apparatus claims 14 of the '374 patent, 13 of the '375 patent, and 22 of the '376 patent (and apparatus claims 15-18 of the '374 patent, 14 and 16 of the '375 patent, and 23, 26-28 of the '376 patent, which are dependent on those claims) ("the Asserted Apparatus Claims"). Each of these independent claims contains two terms that the parties agree are in means plus function form, one from the "means for decoding" family and one from the "means for using" family, labeled as Terms 3, 4, 5, 7, and 8 in the Court's handout at the *Markman* hearing:

[1] For brevity, this brief will cite to the '374 patent only to refer to the common specification.

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- "means for decoding at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a group of macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode" '376 Patent, claim 22 (Term 3)

- "means for decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode" '374 Patent, claim 14 (Term 4)

- "means for selectively decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode" '375 Patent, claim 13 (Term 5)

- "means for using said plurality of decoded smaller portions to construct a decoded picture" '374 Patent, claim 14; '375 Patent, claim 13 (Term 7)

- "means for using said plurality of decoded processing blocks to construct a decoded picture" '376 Patent, claim 22 (Term 8)

The patents' common specification gives a high-level overview of digital video and standard methods for digital video coding. *See* '374 patent, at 1:24 – 2:48. The patents note that a picture in a digital video sequence can be treated either as a "frame" comprising the consecutive lines of the picture or as two "fields" – a "top field" comprising the odd-numbered lines of the picture and a "bottom field" comprising the even-numbered lines of the picture. '374 patent, at 1:42-58. As the patents summarize the invention, "[t]he method entails encoding and decoding each of the macroblocks in each picture in said stream of pictures in either frame mode or in field mode." '374 patent, at 2:58-60. In "field mode," the lines in each macroblock are rearranged to put even lines together and odd lines together. '374 patent, col. 7, lines 54-67. The patents describe encoding the even lines separately from the odd lines in field mode. '374 patent, col. 7, lines 57-58. Figure 8 shows the input and output of the rearranging process in field mode for a pair of macroblocks:

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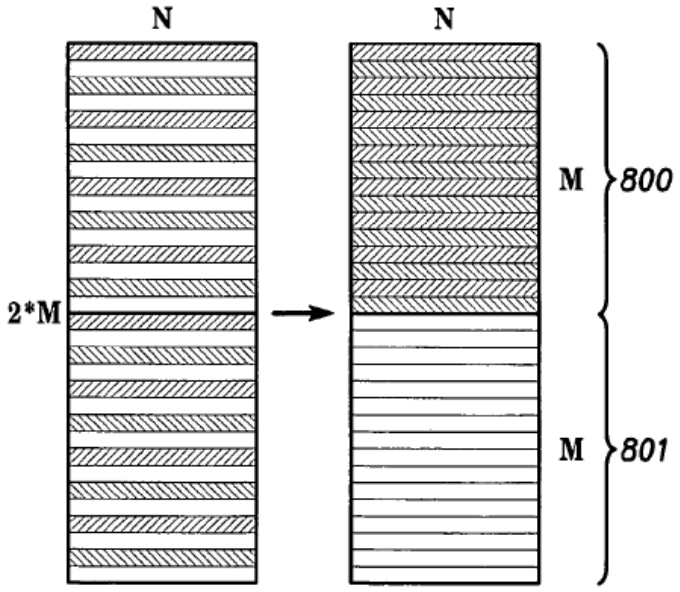

FIG. 8

Conversely, in frame mode, the even and odd lines remain interleaved and are encoded together. '374 patent, col. 7, lines 46-50. The common specification does not explain how the encoder selects between frame mode and field mode but suggests that this decision is based on the mode that will perform better for the content being encoded. '374 patent, at 4:29-34, 6:40-42, 6:50–55. The patents explain that selecting between frame mode and field mode on this basis had been done in the prior art on a picture-by-picture basis. '374 patent, at 4:17-34. The common specification then states that the invention allows making this selection for individual components within a picture, such as macroblocks: "[t]he present invention extends the concept of picture level AFF [adaptive frame/field coding] to macroblocks." '374 patent, at 4:20-21.

After deciding whether to separate the even and odd lines, the patents describe further processing the blocks within the macroblocks using prediction. *See e.g.*, '374 patent, col. 9, lines 38-40. Prediction entails comparing the current block with blocks that have already been encoded to take advantage of redundancies. '374 patent, col. 2, lines 26-41. After first encoding the macroblock or set of macroblocks (e.g., pairs or groups of macroblocks) as frame

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or field macroblocks, prediction is performed on the blocks within the field or frame macroblocks. *See, e.g.*, '374 patent, col. 7, lines 46-58 (macroblock pair); col. 8, lines 30-40 (group of 4 macroblocks).

The common specification describes different types of general purpose computing hardware that can be used to encode or decode digital video. '374 patent, at 4:59-64. In particular, the specification discloses that "[t]he encoder or decoder can be" one of the following (*id.*):

- "a processor": Disclosing a processor obviously just discloses using a general purpose processor to perform decoding, not specific structure.
- "application specific integrated circuit (ASIC)": An ASIC or "application specific integrated circuit" is a general term for an integrated circuit created for a specific application or use.[2] In other words, by disclosing an ASIC, the patents are referring to an unidentified circuit designed to encode or decode in some unidentified way. *See Dictionary of Computer and Internet Terms* 31 (8th ed. 2003) (Decl. of Douglas I. Lewis in Support of Microsoft's Motion for Summary Judgment ("Lewis Decl."), Ex. 2) ("ASIC (Application Specific Integrated Circuit) an integrated circuit (silicon chip) specifically made for a particular complete piece of electronic equipment.")[3].
- "field programmable gate array (FPGA)": FPGAs are similar to ASICs in that they are a programmable hardware chip,[4] and by citing FPGAs, the specification identifies a general type of hardware that can be programmed or modified to perform many different algorithms without saying how one would program that device.
- "coder/decoder (CODEC)": A "coder/decoder (CODEC)" is merely a functional description of the combination of an encoder with a decoder and does not identify a particular implementation of a decoder or any algorithm for encoding or decoding. *Microsoft Computer Dictionary* 106 (5th ed. 2002)

[2] An analogy would be disclosing "paper." Paper can be money, or it can be a novel (or many other things). But disclosing paper does not disclose money.

[3] *See also Microsoft Computer Dictionary* 37, 232 (5th ed. 2002) (Lewis Decl., Ex. 1) (cross-referencing ASIC to "gate array n. A special type of chip that starts out as a nonspecific collection of logic gates. Late in the manufacturing process, a layer is added to connect the gates for a specific function. By changing the pattern of connections, the manufacturer can make the chip suitable for many needs.")

[4] "FPGA n. Acronym for Field Programmable Gate Array. A type of programmable logic chip that can be configured for a wide range of specialized applications after manufacture and delivery." *Microsoft Computer Dictionary* 223 (5th ed. 2002).

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("Hardware or software that can compress and uncompress audio or video data").

- "digital signal processor (DSP)": A digital signal processor (DSP) is a programmable processor, albeit designed for signal processing, *i.e.*, an "integrated circuit designed for high-speed data manipulation and used in audio, communications, image manipulation, and other data acquisition and data control applications." *Microsoft Computer Dictionary* 159.

- "some other electronic device capable of encoding the stream of pictures": This statement in the specification obviously does not disclose sufficiently specific structure to avoid having to disclose an algorithm. This statement just says to use some unidentified electronics.

Each of these listed devices can perform any one of a large number of algorithms for encoding or decoding digital video as well as many other functions. Indeed, the Federal Circuit has required an algorithm for a means element corresponding to an ASIC or an FPGA. *In re Aoyama*, 656 F.3d 1293, 1297-98, 1303 (Fed. Cir. 2011).[5]

II. SUMMARY JUDGMENT IS APPROPRIATE BECAUSE THE DISPUTE IS LEGAL NOT FACTUAL

Summary judgment is appropriate where, as here, "there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a); *see also Celotex Corp. v. Catrett*, 477 U.S. 317, 322 (1986); *Galen v. Cnty. of L.A.*, 477 F.3d 652, 658 (9th Cir. 2007). As the moving party, Microsoft bears the initial burden of showing there is no genuine issue of material fact and that it is entitled to prevail as a matter of law. *Celotex*, 477 U.S. at 323. After Microsoft meets that burden, MMI "must make a showing sufficient to establish a genuine dispute of material fact regarding the existence of the essential elements of his case that he must prove at trial" in order to withstand summary judgment. *Galen*, 477 F.3d at 658. The court is "required to view the facts and draw reasonable

[5] The Federal Circuit found the claims unpatentable because the specification did not disclose an algorithm. *Id.* at 1297-98, 1303 (quoting the patent specification as disclosing both "an application specific integrated circuit, [and] a field programmable gate array").

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inferences in the light most favorable to the [non-moving] party." *Scott v. Harris*, 550 U.S. 372, 378 (2007).

Here, the only issue is one of law, making summary judgment appropriate. Invalidity for failing to disclose structure under Section 112, ¶ 6 is an issue of law. *See Biomedino, LLC v. Waters Technologies Corp.*, 490 F.3d 946, 949 (Fed. Cir. 2007). The failure to disclose structure corresponding to a means plus function claim element invalidates a claim under Section 112, ¶ 2. *Id.* "35 U.S.C. § 112, ¶ 2 requires that claims 'particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention.' For means-plus-function elements, which are statutorily limited to the 'corresponding structure, material, or acts described in the specification and equivalents thereof,' 35 U.S.C. § 112, ¶ 6, section 112, ¶ 2 requires that the specification must permit one of ordinary skill in the art to 'know and understand what structure corresponds to the means limitation.'" *Finisar Corp. v. DirecTV Group, Inc.*, 523 F. 3d 1323, 1340 (Fed. Cir. 2008).

Microsoft asks the Court to grant it summary judgment that the Asserted Apparatus Claims are invalid for indefiniteness because the patents' common specification discloses only general purpose computing hardware and lacks any disclosure of an algorithm for performing the "decoding" and "using" functions.

III. THE PATENT'S COMMON SPECIFICATION DOES NOT DISCLOSE AN ALGORITHM FOR PERFORMING THE DECODING FUNCTION IN THE MEANS ELEMENTS

"The first step in the construction of a means-plus-function claim element is to identify the particular claimed function." *Medical Instrumentation and Diagnostics v. Elekta*, 344 F.3d 1205, 1210 (Fed. Cir. 2003). Here, the parties have agreed on the claimed functions for Terms 3, 4, 5, 7, and 8. *See* Mar. 9 2011, *Markman* Hr'g Tr. at 4:12 – 5:9. Each of Terms 3, 4, and 5

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recites "decoding" as the claimed function.[6] In the "means for using" terms, Terms 7 and 8, the claimed function similarly involves decoding – "using said plurality of decoded smaller portions [or processing blocks] to construct a decoded picture." (emphasis added). Each of the asserted independent apparatus claims contains a version of each type of term, rendering the Asserted Apparatus Claims invalid if either the "means for decoding" or "means for using" element lacks a sufficient disclosed structure or algorithm.

"The second step in the [means plus function claim] analysis is to look to the specification and identify the corresponding structure for that function." *Medical Instrumentation*, 344 F.3d at 1210. The "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id.* (quoting *B. Braun Med. Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed.Cir. 1997)). Moreover, "the corresponding structure for a § 112 ¶ 6 claim for a computer-implemented function is the algorithm disclosed in the specification." *Aristocrat Techs. Austl. PTY Ltd. V Int'l Game Tech*, 521 F.3d 1328 at 1333, *quoting Harris Corp. v. Ericsson Inc.*, 417 F.3d 1241, 1249 (Fed. Cir. 2005). As explained below, the common specification does not disclose an algorithm for performing the claimed "decoding" or "using" functions. A patent that fails to disclose an algorithm for a computer-implemented function is invalid for "lack[ing] sufficient disclosure of structure under 35 U.S.C. § 112 ¶ 6 and [is] therefore indefinite under 35 U.S.C. § 112 ¶ 2." *Aristocrat*, 521 F.3d at 1338.

[6] In the context of the method step that is identical to the claimed function, the parties agreed that the function means "decoding more than one macroblock together in frame coding mode and more than one macroblock together in field coding mode." *See* Mar. 9, 2012 *Markman* Hr'g Tr. 4:17-25.

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1. A "decoder" is not a specific structure.

MMI proposes a "decoder and its equivalents" as structure corresponding to both the "decoding" and "using" means elements in an attempt to avoid the algorithm requirement. MMI Resp. Br. at 9-10; Mar. 9, 2012 *Markman* Hr'g Tr. 8:20-24. The common specification and MMI's pleadings, however, explicitly use the term "decoder" in a functional manner to describe all structures that have "decoding" functionality.

Importantly, the common specification never says that a decoder is a specific structure and indeed, says the opposite, defining "decoder" as "all electronic devices that decode digital video content." *See* '374 patent, 5:1-3 ("The term 'decoder' will be used to refer expansively to all electronic devices that decode digital video content comprising a stream of pictures."). The specification does not use the term "decoder" to identify a specific structure.

MMI also defines "decoder" functionally in its pleadings. Although MMI inconsistently contends that the "decoder" is a specific structure (Mar. 9, 2012 *Markman* Hr'g Tr. 8:20-23), its other arguments show that it intends "decoder" to include any structure that decodes, including general purpose processors. MMI Resp. Br. at 9-10 ("While a decoder 'can be a processor,' it is most accurately described as an 'electronic device that is capable of [decoding] the stream of pictures.'") (quoting ECF No. 159-1, Ex. A ('374 patent), at 4:59-60).[7] Although Mr. Jenner, at the *Markman* hearing, said that a decoder is a specific structure (Mar. 9, 2012 *Markman* Hr'g Tr. 8:20-23), MMI has pointed to no evidence of that, including in its claim construction briefs where it made the same unsupported statement. *See* MMI Opening Br. at 14; MMI Resp. Br. at 9.[8] MMI even admits that it intends a "decoder" to mean

[7] MMI uses brackets to modify the quote from the specification. The common specification says a "device that is capable of *encoding*," not decoding. '374 patent at 4:62-64 (emphasis added).

[8] For this reason, MMI's argument that the cases require an algorithm only when "the ***only*** structure identified for performing the claimed function in those cases was a microprocessor or general purpose computer" (MMI Resp.

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any electronic device "capable of [decoding] the stream of pictures" (MMI Resp. Br. at 10), which shows that MMI seeks to define these means elements purely functionally.

Looking at the accused products also shows how MMI tries to have it both ways by arguing that a "decoder" is a specific structure while reading these means elements to include using a general purpose processor.[9] If the Asserted Apparatus Claims cover software running on a general purpose processor as MMI alleges, the means elements require an algorithm. MMI accuses Windows 7 and Internet Explorer 9 of infringing, which are software programs that run on a general purpose processor, demonstrating MMI's reading of these means elements to include general purpose processors. *See e.g.*, Motorola's Second Amended Disclosure of Asserted Claims and Infringement Contentions, Tab A at 62 (Lewis Decl., Ex. 4) ("The each of the Accused Microsoft Products [*i.e.*, Windows 7 and Internet Explorer 9] includes software that is designed to decode according to the claim language (e.g., the H.264 video decoder software running on a processor performs the claimed function).").

The law does not allow MMI to define these means plus function elements by their function. "The indicated structure must limit the claim so as not to allow pure functional claiming." *Dealertrack v. Huber*, _ F. 3d _, slip op. at 26 (Fed. Cir. 2012). "The point of the requirement that the patentee disclose particular structure in the specification and that the scope of the patent claims be limited to that structure and its equivalents is to avoid pure functional claiming." *Aristocrat*, 521. F.3d at 1333. Indeed, MMI reargues the patentee's

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Br. at 9 (emphasis in original)) is inapposite. Here, "the ***only*** structure" identified for the decoding function is a list of general purpose devices. *See supra* section I. Moreover, even if MMI were correct that the specification disclosed a specific structure, the means plus function elements would cover that structure only and would not reach a general purpose computing device unless the specification disclosed a corresponding algorithm (and then would be limited to using the disclosed algorithm). *Medical Instrumentation and Diagnostics v. Elekta*, 344 F.3d 1205, 1219-20 (Fed. Cir. 2003).

[9] If "decoder" was really limited to a specific structure, Microsoft would not infringe because its Windows 7 and Internet Explorer 9 software runs on a general purpose processor.

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rejected argument in *Aristocrat* in that MMI "is in essence arguing for pure functional claiming as long as the function is performed by a general purpose computer. This court's cases flatly reject that position." *Aristocrat*, 521 F.3d at 1336.

Contrary to MMI's assertion that a "decoder" is a specific structure, the patents identify only general purpose hardware as performing the "decoding" function. The patents say that "[t]he encoder or decoder can be a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), digital signal processor (DSP), or some other electronic device that is capable of encoding the stream of pictures." '374 patent, 4:59-64. As explained above, each of these structures is a unspecified implementation. For this reason, the common specification must disclose an algorithm to avoid invalidity for indefiniteness.

2. The Patents Do Not Disclose An Algorithm For Performing The Claimed Decoding Function

"[A] means-plus-function claim element for which the only disclosed structure is a general purpose computer is invalid if the specification fails to disclose an algorithm for performing the claimed function." *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359,1367 (Fed. Cir. 2008). The common specification identifies no algorithm that describes how to perform decoding. In fact, MMI has never purported to identify such an algorithm, either in its claim construction briefs, at the hearing, or in its infringement contentions. In addition, the common specification identifies no algorithm that describes how to perform the function of "using said plurality of decoded smaller portions [or processing blocks] to construct a decoded picture." With no algorithm disclosed, the Asserted Apparatus Claims are invalid for indefiniteness.

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As explained above, each of the means elements at issue has a claimed function that includes decoding. *See* Terms 3, 4, 5, 7, and 8. But the common specification discloses decoding only at a very high level, literally just saying that one could decode previously encoded video. The specification must "do more than parrot the recited function; it had to describe a means for achieving a particular outcome, not merely the outcome itself." *HTC Corp. v. IPCom GmBH & CO.*, _ F.3d _, slip op. at 18 (Fed. Cir. Jan. 30, 2012). The entirety of the "decoding" disclosed in the common specification is at the following locations: '374 patent, 1:16-17; 1:24-29; 1:59-63; 2:9-14; 2:52-60; 4:54 – 5:3; 15:64 – 16:63. Indeed, decoding is not mentioned after the beginning of column 5 until column 15.

While the last citation above contains somewhat more detail about decoding than the rest of the patent, it does not describe the claimed function of decoding content in frame/field coding mode or of using the decoded portions to construct the decoded picture. This section of the specification says nothing about decoding adaptive frame/field coding, which is part of the claimed "decoding" function,[10] or using the results of that step to construct a decoded picture. *See e.g.*, Term 3 ("that is encoded in field mode" and "that is encoded in frame mode"); Term 7 ("using said plurality of decoded smaller portions to construct a decoded picture"). Instead, this section discusses how to determine "neighboring" blocks in various "prediction modes," where the neighboring block is part of a different macroblock. '374 patent, 15:64 –16:63. Decoding of prediction modes is done before the claimed functions of field/frame decoding and constructing a decoded picture (*see* MMI Mar. 9, 2012 *Markman* tutorial, slide 29 (Lewis Decl., Ex. 5), frame/field decoding occurs after and to right of the "inverse prediction" block;

[10] MMI appears to agree that the "decoding" function requires decoding multiple frame and field macroblocks because it proposed, and Microsoft agreed to, construing the method step that is identical to the decoding function as "decoding more than one macroblock together in frame coding mode and more than one macroblock together in field coding mode." *See* Mar. 9, 2012 *Markman* Hr'g Tr. 4:17-25.

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Mar. 9, 2012 *Markman* Hr'g Tr. at 19:15-22), with prediction mode separately claimed in claims dependent on those with the means elements at issue here. *See* '374 patent, claims 15-18; '375 patent, claims 14. Moreover, by its own terms, this section applies to decoding "macroblock pairs only." '374 patent, 15:64. The claims, however, apply to two or more macroblocks.[11] In addition, the specification quoted above says nothing about the function of the "means for using" terms, Terms 7 and 8, which requires "using said plurality of decoded [smaller portions (Term 7) or processing blocks (Term 8)] to construct a decoded picture." In sum, nothing in the specification provides an algorithm for either the "means for decoding" or "means for using" elements.

IV. TO DATE, MMI HAS NEVER IDENTIFIED AN ALGORITHM FOR PERFORMING THE CLAIMED FUNCTIONS

Although MMI has never identified an algorithm supposedly corresponding to the "decoding" and "using" means elements, MMI's counsel stated at the *Markman* hearing that MMI was "prepared to provide to the court information about where algorithms may be found." Mar. 9, 2012 *Markman* Hr'g Tr. at 9:8-9. Despite counsel's statement, MMI did not identify any algorithm at the hearing. And MMI, even though it had the opportunity to do so, did not identify any such algorithm in its *Markman* briefing. *See* MMI Opening Br. at 13-21, MMI Resp. Br. at 9-11. Indeed, MMI has never identified an algorithm to Microsoft, and Microsoft has no idea what MMI will invent in its opposition to this motion and therefore cannot discuss such contentions here. Consequently, Microsoft will, by necessity, have to respond to any contentions relating to newly located algorithms in its reply brief to this motion.

[11] The claims define "smaller portions" as "ha[ving] a size that is larger than one macroblock" – i.e., each "smaller portions" is comprised of a pair or larger group of macroblocks. *See* '374 Patent, at cl. 14; '375 Patent, at cl. 13). Similarly, "processing blocks" are claimed as "containing a pair of macroblocks or a group of macroblocks." '376 Patent, at cl. 22.

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V. CONCLUSION

The patents in suit describe only general purpose devices for implementing the decoding function. The patents disclose no algorithm for decoding. For these reasons, the Asserted Apparatus Claims are invalid under 35 U.S.C. § 112, ¶ 2 for indefiniteness.

DATED this 22nd day of March, 2012.

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CERTIFICATE OF SERVICE

I hereby certify that on March 22, 2012, I electronically filed the foregoing document with the Clerk of the Court using the CM/ECF system, which will send notification of such filing to the following:

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